CLAIMS

What is claimed is:

1. An output stage for an amplifier, comprising:

an input buffer that receives an input signal; and

a clamp buffer that receives a clamp signal, the clamp buffer being coupled to the input buffer;

one of the input buffer and the clamp buffer biasing an associated output portion of the output stage to provide an output signal depending on the input signal relative to the clamp signal.

2. The output stage of claim 1, the output portion provides the output signal based on the input signal when the output stage operates in a normal mode and provides the output signal based on the clamp signal when the output stage operates in a clamping mode, the mode depending on the level of the input signal relative to the clamp signal.

3. The output stage of claim 1, further comprising a differential pair of components that couples the input buffer with the clamp buffer, the differential pair controls which of the input buffer and the clamp buffer biases the output portion.

4. The output stage of claim 3, one of the differential pair of components being part of the input buffer and another of the differential pair of components being part of the clamp buffer, the differential pair of components controls which of the input buffer and the clamp buffer biases the output portion.

5. The output stage of claim 3, the differential pair operates to disable the input buffer during a clamping mode based on the input signal being within a clamping range established by the clamp signal, such that a feedback loop that includes the output portion and the input buffer is broken during the clamping mode.

6. The output stage of claim 3 further comprising a bias network coupled to receive a bias signal from the one of the input buffer and the clamp buffer that is biasing the output portion, the bias network is coupled to bias the output portion of the output stage based on the bias signal.

7. The output stage of claim 6, the bias network comprising a current mirror network.

8. The output stage of claim 6, the differential pair of components further comprising transistors, each having a common emitter that is coupled to bias the bias network based on a relative level of the input signal and the clamp signal.

9. The output stage of claim 6, the output portion further comprising an output circuit that provides the output signal based on the biasing implemented by the bias network.

10. The output stage of claim 9, the output circuit comprising at least one transistor biased by the bias network to provide at least a portion of the output signal.

11. The output stage of claim 1, the clamp buffer comprising first and second buffer systems coupled to the input buffer, each of the first and second buffer systems is coupled to receive respective first and second clamp signals for biasing the output portion during a respective clamping mode, the output stage operating in a respective one of the clamping modes depending on the input signal relative to each of the first and second clamp signals.

12. The output stage of claim 11, the input buffer comprising plural transistors in a diamond follower arrangement, each of the first and second buffer systems comprising plural transistors in a diamond follower arrangement, at least one of the transistors of the first buffer system and the input buffer are shared, and at least one of the transistors of the second buffer system and the input buffer are shared, whereby biasing the output portion during first and second clamping modes is facilitated.

13. The output stage of claim 1, the clamp buffer further comprising a dynamic buffer that provides a dynamic buffer output signal for biasing the output portion during a clamping mode as a function of a load connected at the output.

14. An amplifier system implementing the output stage of claim 1, the amplifier system comprising:

a preceding amplifier stage that amplifies a signal received thereby according to an associated gain and provides the input signal to the output stage.

15. An integrated circuit comprising the amplifier system of claim 14.

16. An amplifier system comprising:

an input buffer that provides a first bias signal based on an input signal received by the input buffer; and

at least one clamp buffer associated with the input buffer and provides a second bias signal based on a clamp signal;

a bias network coupled to the input buffer and to the at least one clamp buffer;

an output circuit coupled to the bias network, the bias network biases the output circuit to provide an output signal based on the first bias signal when the system operates in the a normal operating mode, and biasing the output circuit to provide the output signal based on the second bias signal when the system operates in a clamping mode, the operating mode is based on the input signal relative to the clamp signal.

17. The system of claim 16, the bias network further comprising at least one current mirror.

18. The system of claim 16, further comprising at least one preceding amplifier stage coupled to provide the input signal to the input buffer.

19. An integrated circuit comprising the amplifier system of claim 16.

20. The system of claim 16, the output circuit further comprising at least one output transistor, the at least one clamp buffer including at least one transistor that is substantially smaller than the at least one output transistor of the output circuit, whereby switching between the normal and clamping operating modes is facilitated.

21. The system of claim 16, further comprising a control network that includes at least one component from the input buffer and at least one component from the at least one clamp buffer, the control network enabling one of the input buffer and the at least one clamp buffer to provide the respective bias signal to the bias network based on the input signal relative to the clamp signal.

22. The system of claim 21, the control network further comprising a differential pair of transistors that couples the input buffer with the at least one clamp buffer, the differential pair controls which of the input buffer and the at least one clamp buffer biases the bias network based on the input signal relative to the clamp signal.

23. The system of claim 16, the clamp buffer comprising first and second buffer systems coupled with the input buffer, each of the first and second buffer systems is coupled to receive a respective one of first and second clamp signals to control the bias network to bias the output in a respective clamping mode depending on the input signal relative to each of the first and second clamp signals.

24. The system of claim 23, the input buffer comprising plural transistors in a diamond follower arrangement, each of the first and second buffer systems comprising plural transistors in a diamond follower arrangement, the first buffer system and the input buffer share at least one transistor, and the second buffer system and the input buffer share at least one transistor, whereby biasing during first and second clamping modes is facilitated.

25. The system of claim 16, the at least one clamp buffer further comprising a dynamic buffer portion that provides a dynamic buffer output signal as a function of a load connected at the output, the at least one clamp buffer dynamically biases the bias network during the clamping mode based on the dynamic buffer output signal.

26. An amplifier system comprising:

first means for, during a normal operating mode, buffering an amplifier input signal to bias an associated output portion of the amplifier system based on the amplifier input signal;

second means for, during a clamp operating mode, buffering at least one clamp input signal to bias the associated output portion based on the clamp input signal; and

means for controlling which of the normal and clamp operating modes is implemented based on the amplifier input signal relative to the at least one clamp input signal, the means for controlling being coupled to the first means for buffering and to the second means for buffering to enable biasing of the associated output portion according to the operating mode.

27. The amplifier system of claim 26, further comprising means for biasing the output portion of the amplifier system based on the mode being implemented by the means for controlling.

28. The amplifier system of claim 26, further comprising means for varying the biasing provided by the second means for buffering during the clamping mode based on a load connected to the output portion.

29. A method for amplifying an input signal comprising:

receiving at least one clamp signal at an output stage of an amplifier to set an associated clamping level;

while in normal operating mode, biasing an output portion of the amplifier to provide an amplifier output signal based on the input signal;

while in a clamping mode, biasing the output portion to provide the output signal based on the clamp level; and

controlling the operating mode based on the input signal relative to the clamp level.

30. The method of claim 29, further comprising varying the biasing of the output portion in the clamping mode based on a load connected to the output portion.